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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/678,847	**Applicant(s)** SLEEMAN, PETER T.	
	Examiner Tanh Q. Nguyen	**Art Unit** 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The declaration was filed with the application on October 3, 2003. However, it appears that the declaration was postdated for November 9, 2003.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 6-8 are objected to because of the following informalities: "FIFO buffers" in line 2 of claim 6 should be replaced with "data buffers" to be consistent with the

limitations recited in claims 7-8. Appropriate correction is required.

5. Claims 9-10 are objected to because of the following informalities:

it appears that claim 9 should depend on claim 6 instead of claim 3 - to have proper antecedent basis because claim 9 recites in line 2 and line 3 "each data buffer", implying more than one data buffer, and claim 3 recites a supplementary buffer while claim 6 recites supplementary data buffers;

it also appears that claim 10 should depend on claim 9 instead of claim 3 - to have proper antecedent basis because claim 3 does not recite any "control and status lines"; claim 9 recites "first control and status lines", and claim 10 recites "second control and status lines".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 11-16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bedingfield et al. (USP 5,537,654)** in view of **AAPA (Applicant Admitted Prior Art - specification, page 1, line 21-page 3, line 11; FIG. 1)**.

8. As per claim 1, **Bedingfield** teaches an interface device [PCMCIA modem 100, FIG. 1] for enabling communications between a host [200, FIG. 1] and a subsystem [the

modem], comprising:

a serial interface [a UART that is not shown] configurable to establish a bi-directional serial data communication channel to the subsystem [col. 7, lines 14-22]; and

a parallel interface configurable to establish an auxiliary parallel data communication channel to the subsystem operable in conjunction with the serial data communication channel [col. 7, lines 22-27: a direct transfer from the host computer to PCMCIA modem 100 is a parallel transfer because the host CPU transfers data for transmission over a data communication channel by writing data in parallel [col. 7, lines 14-16]].

Bedingfield, therefore, discloses the claimed invention except for the interface device comprising a register set (for controlling the serial interface) comprising a plurality of registers configurable to control host-subsystem communications according to a UART standard; and a host interface configurable to establish data communication with the host.

AAPA teaches a register set [22, FIG. 1] for controlling a serial interface [UART 20, FIG. 1] comprising a plurality of registers configurable to control host-subsystem communications according to a UART standard [page 1, line 21-page 3, line 11]; and a host interface [12, 14, FIG. 1] configurable to establish data communication with the host.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate AAPA's register set and host interface into Bedingfield's UART - in order to use the register set to control host-subsystem communications and to use the host interface to establish data communication with the host.

9. As per claims 11-16, AAPA teaches the UART standard being the 16550 standard [page 1, line 21];

Bedingfield teaches a PCMCIA modem [100, FIG. 1] including a UART (see rejection to claim 1 above], hence a PCMCIA modem card comprising a UART integrated with a modem [col. 7, lines 14-22];

the combination of Bedingfield and AAPA does not teach the subsystem including wireless interface for communicating with a third party data transceiver. Since PCMCIA wireless cards are well known in the art at the time the invention was made, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the subsystem of Bedingfield's PCMCIA modem to include a wireless interface - in order to communicate with a wireless data transceiver.

Bedingfield teaches a system comprising a host [200, FIG. 1], a subsystem (a modem) and an interface device (UART and parallel interface) connected between the host and the subsystem;

the combination of Bedingfield and AAPA does not teach the serial data communication channel and the auxiliary parallel communication channel including wireless portions. Since PCMCIA wireless cards are well known in the art at the time the invention was made, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the serial data communication channel and the auxiliary parallel communication channel of Bedingfield's PCMCIA modem to include wireless portions - in order to communicate with a wireless data transceiver.

Bedingfield teaches the serial data communication channel and the auxiliary parallel communication channel being made exclusively of fixed links [FIG. 1; col. 7, lines 14-27].

10. As per claim 17, Bedingfield a method for communicating data between a host and a subsystem, comprising:

establishing a bi-directional serial data communication link with the subsystem conforming to a UART standard [col. 7, lines 14-22];

establishing an auxiliary parallel data communication link with the subsystem; and transferring data over the auxiliary parallel data communication link to bypass the serial data communication link [col. 7, lines 22-27].

Bedingfield does not teach a register set conforming to a UART standard. AAPA teaches a register set [22, FIG. 1] for controlling a UART [20, FIG. 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate AAPA's register set into Bedingfield's UART - in order to use the register set to control the UART.

11. Claims 2-10, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bedingfield et al.** in view of **AAPA**, and further in view of **Moss et al. (USP 5,604,870)**.

12. As per claims 2, 18, the combination of Bedingfield and AAPA does not teach the parallel interface operating under control of the register set (or the parallel data communication link being also established under control of the register set). Moss

teaches a parallel interface [FIG. 2] operating under the control of a register set (or a parallel data communication link being established under control of the register set) that provide the look and feel of a UART - from the perspective of the host [col. 3, lines 26-29]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the parallel interface operating under the control of the register set of the UART (or a parallel data communication link being established under control of the register set of the UART) - in order to provide the look and feel of the UART to the host communicating via the parallel interface.

13. As per claims 3-8, the combination of Bedingfield and AAPA does not teach supplementary data buffers for writing and reading data to and from the subsystem via the parallel interface. Moss teaches data buffers [221, 223 - FIG. 2] being used as temporary storage for writing and reading data to and from the subsystem via a parallel interface [col. 6, lines 26-30; col. 7, lines 8-11]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include data buffers, as is taught by Moss, into the combination of Bedingfield and AAPA, in order to provide temporary storage for data being written or read to and from the subsystem via the parallel interface.

Moss further teaches one of the registers [FCR 218, FIG. 2] being mapped to at least one of the data buffers so that accesses to the mapped register will cause accesses to at least one of the data buffers (FCR 218 is a FIFO control register, hence access to FCR 218 will cause access to at least one of the FIFOs (data buffers)), and the data buffers being FIFO buffers [301, FIG. 3; 601, FIG. 6].

14. As per claims 9-10, Moss teaches that FIG. 2 does not depict all the internal control and status interconnections as these are well known in the art [col. 4, lines 62-64], hence implicitly teaches control and status lines connected between each data buffer and the register set to communicate control and status signals to and from each buffer (i.e. control and status signals between the register set and each buffer), and also implicitly teaches control and status lines connected between each data buffer and the parallel interface to communicate control and status signals to and from each buffer (i.e. control and status signals between the parallel interface and each buffer).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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08/05/2005

TQN
August 5, 2005